

What is claimed is:

- 1 1. A method of filtering over-sampled data comprising:
 - 2 a. receiving a word of over-sampled data including a plurality of sample bits
3 for each of a plurality of data bits;
 - 4 b. detecting a sample bit having one logic value and, on either side of it, bits
5 having the opposite logic value; and
 - 6 c. outputting the received word with the sample bit having said one logic value
7 inverted.

- 1 2. The method of claim 1 wherein said step of detecting comprises:
 - 2 a. exclusively ORing each sample bit in said word separately with the next
3 highest and next lowest bits; and
 - 4 b. ANDing the results said ORing.

- 1 3. The method of claim 2 and further including providing a history bit to supply the
2 next highest bit for the most significant bit of said word.

- 1 4. The method according to claim 3 wherein a plurality of words in succession are
2 received, with the steps of claim 1 performed for each word, and further including
3 saving the least significant bit of a last previous word received as the history bit for
4 the next word received.

- 1 5. The method according to claim 4 comprising receiving words until the end of a
2 packet is reached.

- 1 6. The method of claim 2 wherein said step of outputting comprises outputting each of
2 said sample bits uninverted if the result of said ANDing is one logic level and
3 inverted if the result is the other logic level.

- 1 7. The method according to claim 1 comprising receiving said word from an over-
2 sampler.
- 1 8. The method according to claim 7 and further comprising selecting a word to be
2 received from between two over-samplers.
- 1 9. The method according to claim 1 wherein said over-sampled data is USB 2.0 data.
- 1 10. Apparatus for filtering over-sampled data comprising:
2 a. detection logic coupled to receiving a word of over-sampled data including
3 a plurality of sample bits for each of a plurality of data bits and to detect a
4 sample bit having one logic value and on either side of it, bits having the
5 opposite logic value; and
6 b. an output circuit outputting the received word with the sample bit having
7 said one logic value inverted.
- 1 11. The apparatus of claim 10 wherein said detection logic comprises:
2 a. a plurality of terminals for receiving said sample bits for each of a plurality
3 of data bits;
4 b. a plurality of first two input logic circuits to perform an exclusive OR
5 function, each having its inputs coupled to two adjacent terminals; and
6 c. a plurality of second two input logic circuits to perform an AND function,
7 each having as inputs outputs of two adjacent first logic circuits.
- 1 12. The apparatus of claim 11 and further including a storage element to store a history
2 bit, an output of said storage element coupled to one of said first logic circuits
3 having as a second input a sample bit which is most significant.

- 1 13. The apparatus of claim 12 wherein said output circuit comprises:
- 2 a. a plurality of inverters, one coupled to each terminal; and
- 3 b. a plurality of multiplexers, each having a first data input coupled to an
4 output of one of said inverters, an second data input coupled to the
5 corresponding terminal, and a control input coupled to the output of the one
6 of said second logic circuits associated with said terminal and an output.
- 1 14. The apparatus of claim 13 wherein a plurality of words in succession are to be
2 received, said storage element having an input coupled to the least significant
3 sample bit and having a clock input to clock said input to its output prior to
4 receiving a new word.
- 1 15. The apparatus of claim 14 and further comprising an over-sampler to supply said
2 words to said terminals.
- 1 16. The apparatus of claim 15 wherein two over-samplers are provided and further
2 including a selection circuit to select between two over-samplers.
- 1 17. The apparatus of claim 16 wherein said selection circuit is a multiplexer.
- 1 18. The apparatus of claim 13 wherein said over-sampled data is USB 2.0
- 1 19. A computer readable memory containing program instructions that, when executed
2 by a processor, cause the processor to:
- 3 a. receive a word of over-sampled data including a plurality sample bits for
4 each of a plurality of data bits;
- 5 b. detect a sample bit having one logic value and, on either side of it, bits
6 having the opposite logic value; and
- 7 c. output the received word with the sample bit having said one logic value
8 inverted.

- 1 20. A computer readable memory according to claim 19 wherein said processor is
2 caused to
3 a. exclusively OR each sample bit in said word separately with the next
4 highest and next lowest bits; and
5 b. AND the results said exclusive ORing.
- 1 21. A computer readable memory according to claim 20 wherein said processor is
2 caused to provide a history bit to supply the next highest bit for exclusive ORing
3 with the most significant bit of said word.
- 1 22. A computer readable memory according to claim 21 wherein said processor is
2 caused to receive a plurality of words in succession, with the steps of claim 1
3 performed for each word and said processor is further caused to save the least
4 significant bit of a last previous word received as the history bit for the next word
5 received.
- 1 23. A computer readable memory according to claim 22 wherein said processor is
2 caused to receive words until the end of a packet is reached.
- 1 24. A computer readable memory according to claim 23 wherein said processor is
2 caused to output said each sample bits uninverted if the result of said ANDing is
3 one logic level and inverted if the result is the other logic level.
- 1 25. A computer readable memory according to claim 21 wherein said over-sampled
2 data is USB 2.0 data.